HOT-CARRIER CIRCUIT RELIABILITY SIMULATION

ABSTRACT OF THE DISCLOSURE

The present invention is directed to a number of improvements in methods for reliability simulations in aged circuits whose operation has been degraded through hot-carrier or other effects. A plurality of different circuit stress times can be simulated within a single run. Different aging criteria may be used for different circuit blocks, circuit block types, devices, device models and device types. The user may specify the degradation of selected circuit blocks, circuit block types, devices, device models and device types independently of the simulation. Device degradation can be characterized in tables. Continuous degradation levels can be quantized. Techniques are also described for representing the aged device in the netlist as the fresh device augmented with a plurality of independent current sources connected between its terminals to mimic the effects of aging in the device. The use of device model cards with age parameters is also described. To further improve the circuit reliability simulation, a gradual or multi-step aging is used instead of the standard one step aging process. Many of these features can be embedded within the circuit simulator. A user data interface is also presented to implement these techniques and further allow users to enter their device models not presented in the simulator. For example, a proprietary model of, say, the substrate current in an NMOS could used be with a SPICE simulator employing a different model to simulate the aging of the circuit.